THIS NASA INVENTION APPEARS TO HAVE EXCELLENT COMMERCIAL POTENTIAL

NASA CASE NO. MFS-25,535-1

PRINT FIG. 1

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(NASA-Case-MFS-25535-1) THREE PHASE POWER FACTOR CONTROLLER Patent Application (NASA) 17 p HC A02/MF A01 CSCL 09C

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G3/33 39701

NASA Case No. MFS-25535

THREE PHASE POWER FACTOR CONTROLLER

TECHNICAL ABSTRACT

This invention relates to devices for reducing the power input to an unloaded induction type motor, and particularly to an improved device for effecting power reduction in three phase motors employing the technique of power factor control.

As is well known, the inventor in this case previously invented and is the patentee of a system for reducing power consumption by induction motors through the employment of a feedback loop which is dedicated to holding the power factor of a motor constant. While that invention was primarily directed to single phase motors, the invention was also applicable to three-phase motors, particularly those wherein there is a common, or fourth, input power terminal. In order to extend the usefulness of his invention to three-phase motors wherein there is no common input terminal, it was found that something further must be done in order to achieve stable operation. In accordance with this invention, the key to a solution involved two things. First, the frequency of a single phase feedback signal was too low, and this was remedied by employing three phase detectors, e.g., half wave phase detectors 32, 34, and 36, as shown in Fig. 1, which resulted in a feedback control signal of 180 Hz, rather than 60 Hz or 120 Hz, as previously employed. Second, this higher frequency signal was conditioned by a signal conditioner 66 which presented this characteristic: At about 2 Hz, the circuit commenced providing a lag state conditioning which diminished as the value of resistor 76 commenced to have a dominant effect over capacitor 74 of this circuit. Then, at about 20 Hz, capacitor 72 commences to be effective to, again, impose a pronounced lag effect. The resulting signal is a relatively smooth signal, but one wherein the signal will still be responsive to signal changes incident to changes in motor loading. The thus derived conditioned signal is then conventionally employed to vary the turn-on time of SCR devices in circuit with three phase motor 10.

An alternate embodiment of the invention, shown in Fig. 5, employs three full wave phase detectors, and thus the control signal is increased to 360 Hz. This increased frequency requires that the signal conditioning circuitry be varied somewhat, but still basically reacts in the same manner as that described above with respect to Fig. 1.

The nub of the invention in this case was the determination that the frequency of a control signal available from a single phase was too low in order to effect stable control of a three terminal, three phase motor, and then after having remedied this problem as described above, the determination of the necessary signal conditioning characteristic and circuitry sufficient to achieve signal smoothing of the control signal without reducing its responsiveness to signal changes occurring by virtue of changes in motor load.

It is understood that quite a number of manufacturers of power factor controllers have experienced the stability problem referred to above, and it is further understood that at this point, tests of the circuitry of the invention indicated that this invention will provide a solution to their problem.

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EMPLOYER:	NASA-MSFC
APPLICATION S. N.:	199,765
DATE FILED:	October 23, 1980

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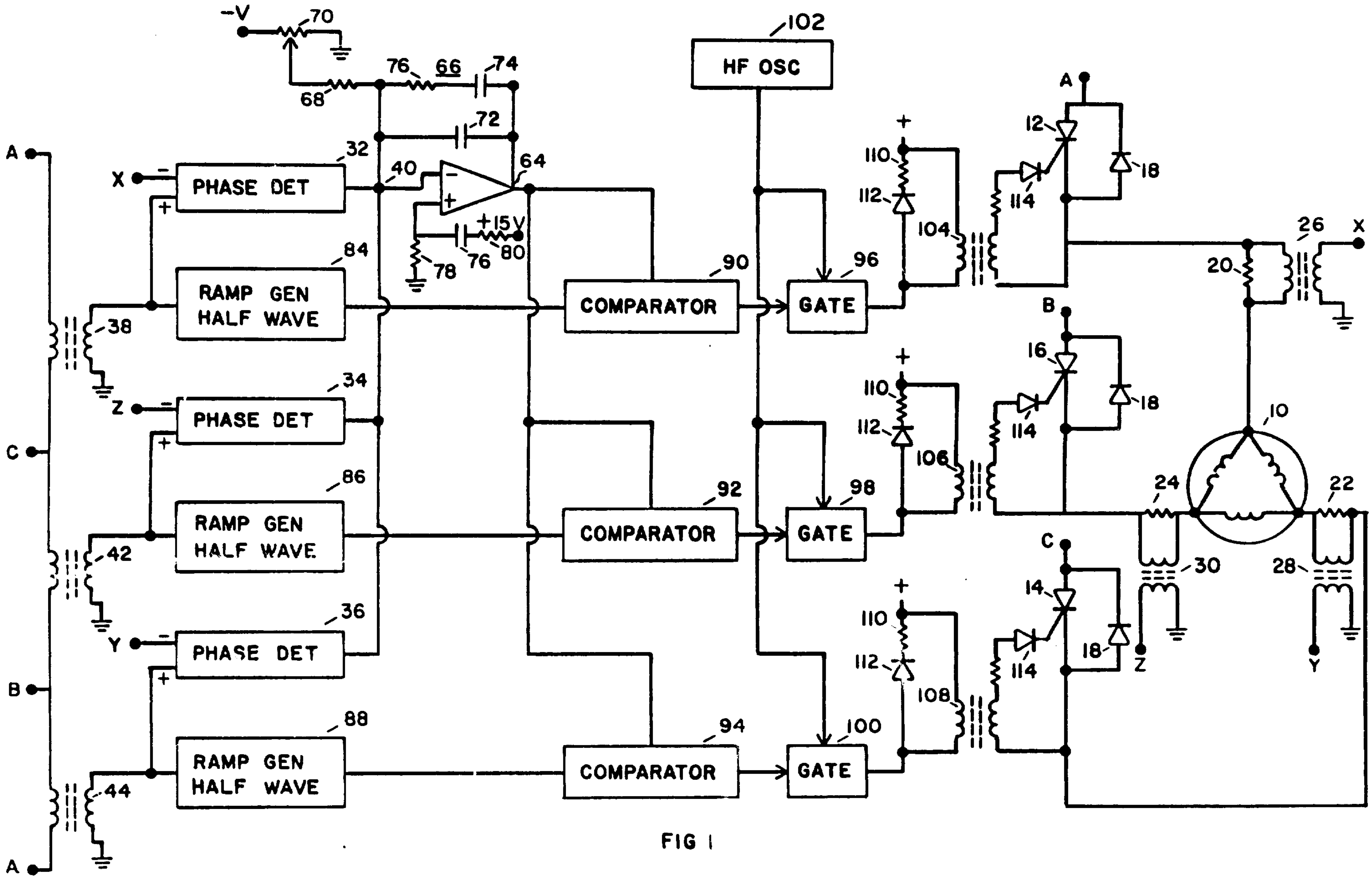

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FIG 1

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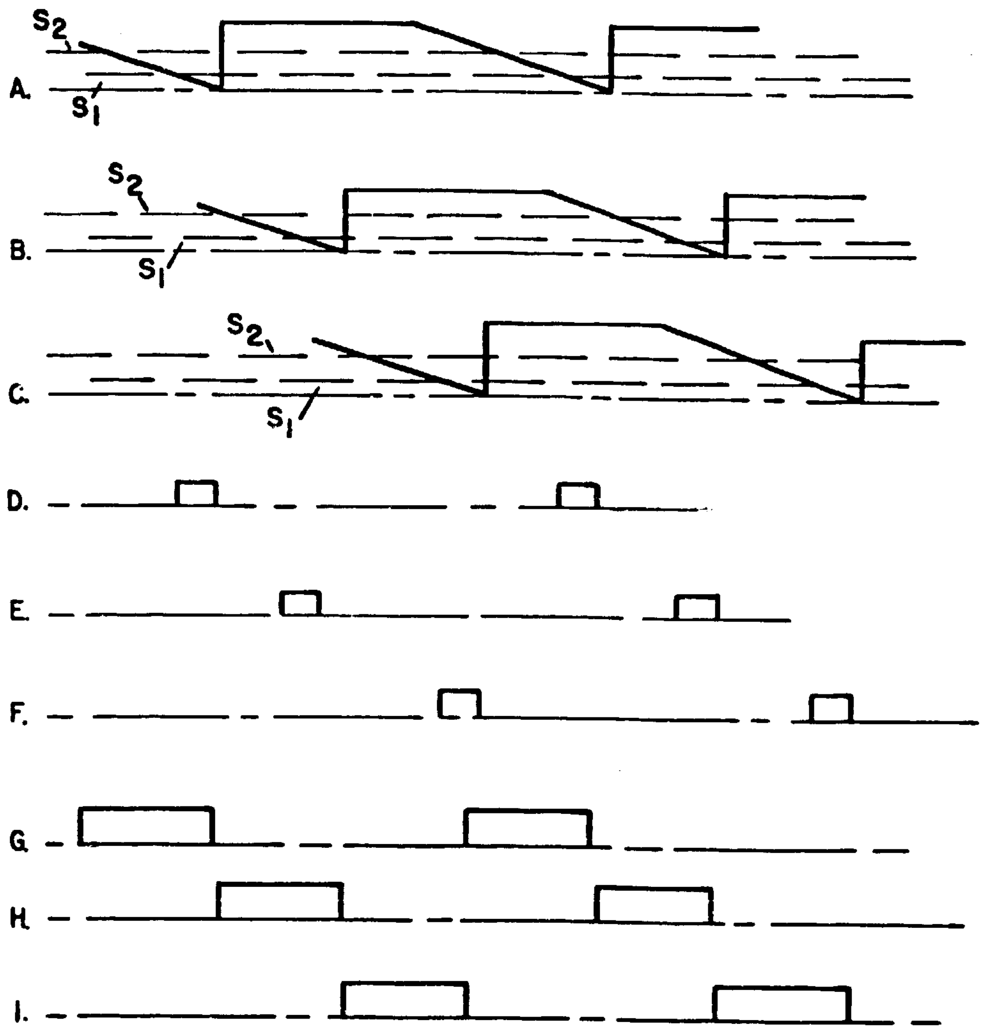

FIG. 4

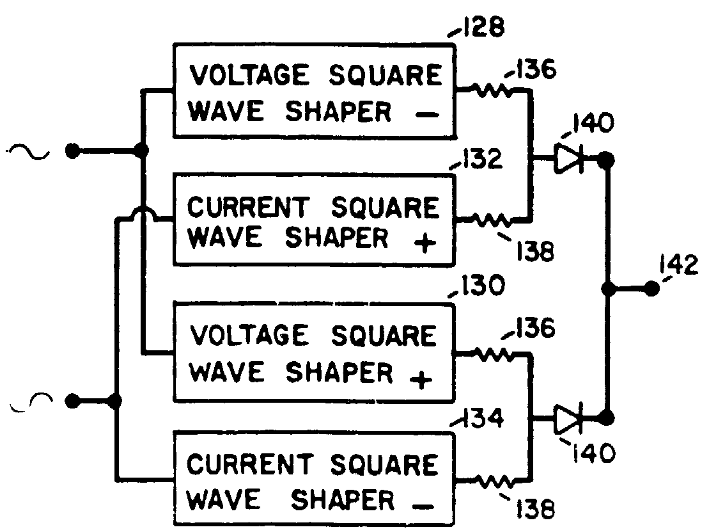

FIG. 6

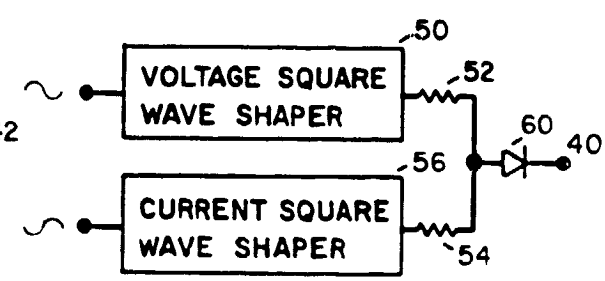

FIG. 2

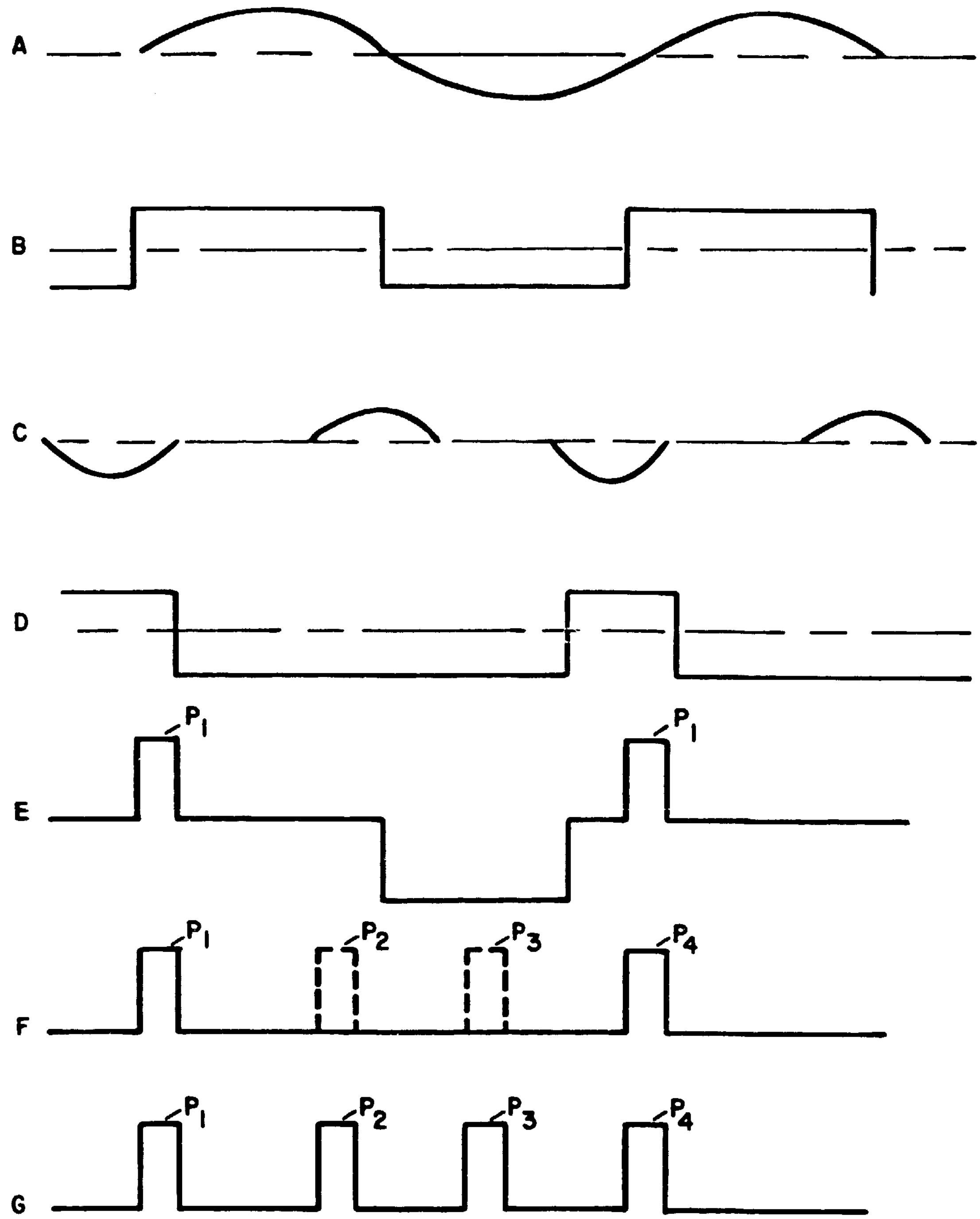

FIG 3

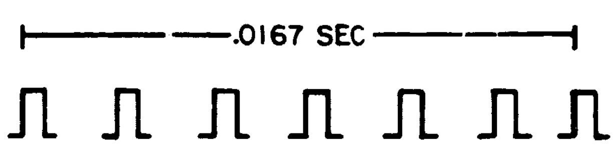

FIG 7

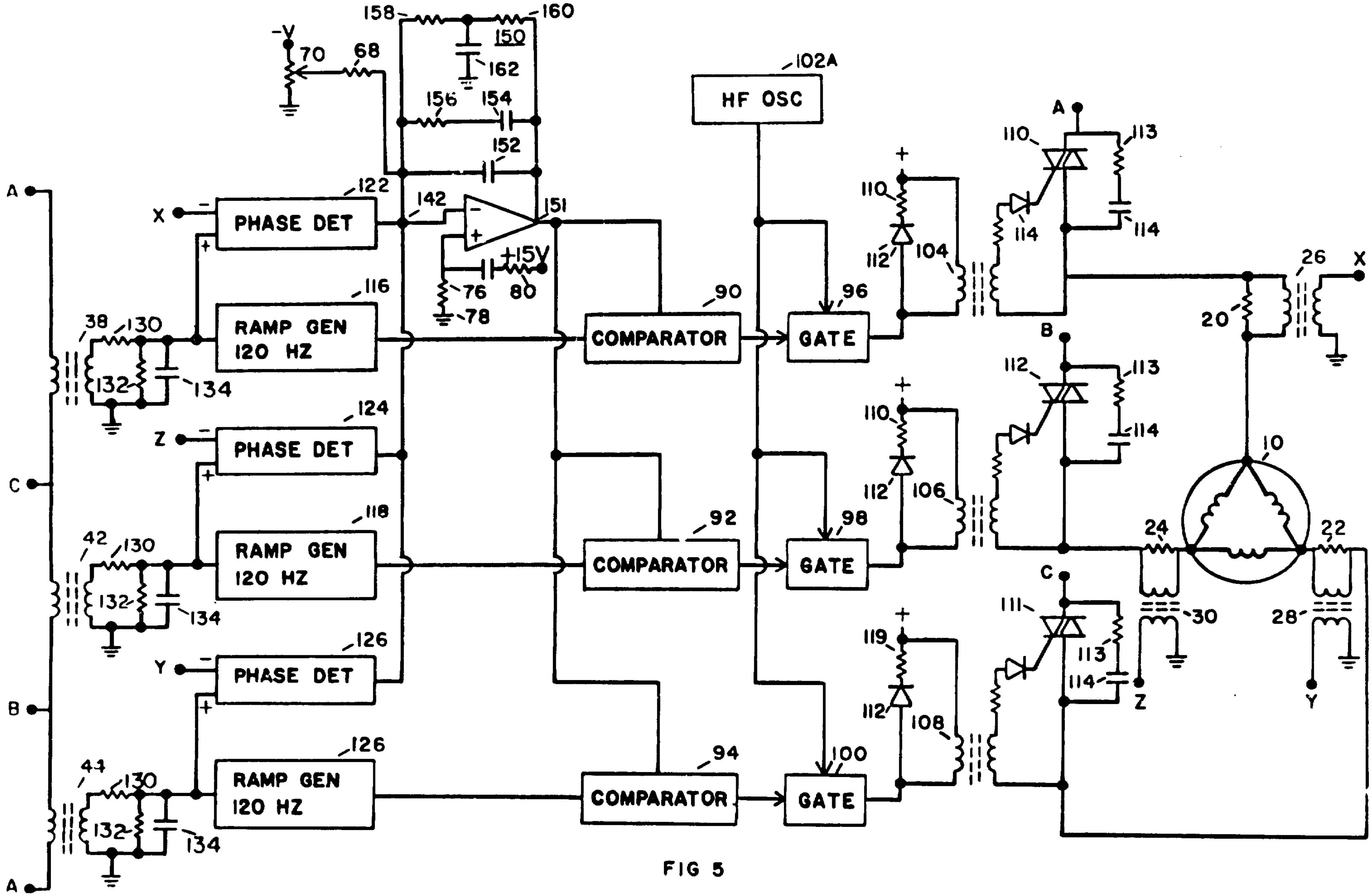

FIG 5

MFS-25,535-1

THREE PHASE POWER FACTOR CONTROLLER

Origin of the Invention

This invention described herein was made by an employee of the United States Government and may be manufactured and used by or for the Government of the United States for governmental purposes and without the payment of any royalties thereon or therefor.

Technical Field

This invention relates to power input controls for induction motors, and particularly to an improved control for regulating power input to a three phase motor as a function of load.

Background Art

The applicant previously described in U. S. Patent 4,052,648 a power reduction system for induction motors in which the effective voltage input to the motor is varied directly as a function of load. In that patent it is noted that the power factor of such motors varies directly with loading, and that the power factor of a less than fully loaded motor might be maintained at an optimum level by reducing the effective voltage to the motor, the applicant earlier determined, and such is described in referenced patent, that power input to a motor may be automatically varied as a function of load by commanding that it operate at a selected power factor. The system described in this patent has been very successful and has been widely used with respect to single phase motors.

The applicant also tested the applicability of this system to three phase motors, testing being of motors wherein the "Y", or common reference power, terminal of the motor is brought out of the motor and available for control purposes. It worked well. In many three phase motors, however, it has been found that a common reference terminal is not available, that is, a common reference terminal through which current from all three phases flow. It further appears that simply sampling one of the three phases of the motor and deriving a power factor control signal from it is not satisfactory. Significant stability problems may be encountered.

It is an object of this invention to provide an improved three phase

power factor controller particularly adaptable for employment with three phase motors wherein there is not available a terminal common to all phases, and wherein problems of motor instability are overcome.

Disclosure of the Invention

In accordance with this invention, a power factor, or phase detector, is employed for each of the phases of a three phase induction motor, and the detected values are summed to effect a composite signal, and this signal is used as a basis of control. The signal is subjected to signal conditioning, including signal integration, and employed to control the turn-on time of each of three thyristors coupling power to the motor.

Brief Description of the Drawings

Fig. 1 is an electrical schematic diagram of an embodiment of the invention.

Fig. 2 is an electrical schematic diagram of the phase detectors employed in the embodiment of the invention shown in Fig. 1.

Fig. 3 consists of a series of waveforms illustrative of the operation of the phase detector shown in Fig. 2.

Fig. 4 consists of a series of waveforms illustrating the generation of triggering pulses in accordance with the circuitry shown in Fig. 1.

Fig. 5 is an electrical schematic diagram of an alternate embodiment of the invention.

Fig. 6 is an electrical schematic diagram of the phase detector employed in the embodiment of the invention shown in Fig. 5.

Fig. 7 consists of a series of signal pulses illustrating the frequency of turn-on of the triac-type thyristors employed in the circuit shown in Fig. 5.

Best Mode For Carrying Out the Invention

Referring initially to Fig. 1, a three phase motor 10 is powered through SCR (silicon control rectifier) devices 12, 14, and 16 from a three phase power line, typically providing 220 or 440 volts, 60 cycle, A.C. from terminals A, B, and C. One phase of such a signal is illustrated by voltage wave a of Fig. 3. As the SCR devices provide for con-

duction only in one direction, a diode 18 is connected across each SCR and poled for opposite direction conduction. Current is sampled by current sampling transformers 26, 28, and 30, shunted by resistors 20, 22, and 24, each of these resistors being connected in series with an input to motor 10. Transformers 26, 28, and 30 are individually connected across one of these resistors (via a primary winding, as shown), and with one secondary terminal grounded, the other secondary terminal provides a discretely phased current signal output (as shown in waveform c of Fig. 3). Terminal X is associated with phase A, terminal Z is associated with phase B, and terminal Y is associated with phase C. A power factor signal, a signal inversely proportional to the current-voltage phase differential of each of the three phase inputs is obtained, separately, by phase detectors 32, 34, and 36. Phase detector 32 receives a current responsive signal sample from terminal X, representative of the A phase current, and a voltage signal from transformer 38, representative of the A-C phase voltage, and provides a first phase detected output on terminal 40. Phase detector 34 receives a sample from terminal Z, representative of the C phase current, and a C-B voltage sample from transformer 42 and provides a second phase detected output on terminal 40. Phase detector 36 receives a phase C current signal sample from terminal Y, and a B-A phase voltage sample from transformer 44 and provides a third phase detection signal on terminal 40. The three signals, designated P_1, P_2, and P_3, respectively, from the three phase detectors are shown in waveforms f and g of Fig. 3.

The phase detectors are identical, and an embodiment of each is shown in Fig. 2. It includes two conventional squaring circuits. One is voltage square wave shaper 50, which provides through resistor 52 a rectangular wave (waveform b of Fig. 3) responsive to the input voltage (waveform a of Fig. 3). The second one is current square wave shaper 56, which provides through resistor 54 a rectangular wave (waveform d of Fig. 3), representative of the negative half cycle of input current (waveform c of Fig. 3). This output of phase detection is also noted by the $\pm$ signs at the input terminals of the phase detectors (as shown in Fig. 1). The outputs of the two wave shaping circuits are combined through resistors 52 and 54. Diode 60 passes only the positive portion of each output to terminal 40, which is common with the outputs of phase detectors 32, 34, and 36 (as

shown in Fig. 1). Waveform e illustrates the combination process showing the waveform of a single phase detector as it would appear without diode 60, which diode eliminates the negative portions of the waveforms. Significantly, in the detection process, each phase detector produces a pulse (e.g., P_1 from detector 32, P_2 from detector 34, and P_3 from detector 36) which is, in effect, turned "on" by the leading or rising edge of voltage waveform b and turned "off" by the trailing edge of waveform d. Thus, the width of pulse P_1 (it has a constant amplitude) tends to increase upon the occurrence of increased phase angle between current and voltage (thus decreased power factor) and decrease in width with decreased phase angle (and thus increased power factor).

Assuming as indicated that pulse P_1 represents the output of phase detector 32, waveforms f and g illustrate the relatively time presence of output pulses P_2 and P_3 from phase detectors 34 and 36, respectively. As the outputs are brought together at terminal 40, waveform g of Fig. 3 illustrates the combined signals at this point. This composite of these becomes the basic feedback control signal, and as will be noted, this is a signal of pulses of a repetition rate of 180 Hz. This is in contrast to previous circuit approaches wherein a single phase detected output (from one of the three phases) is employed, which would, of course, have been either at 60 Hz or 120 Hz rate, depending upon whether a half or full wave detection was employed.

The next step in accordance with this invention is to effect a signal conditioning of the control signal wherein the direct current character of the signal must be compatible with the thyristor trigger circuitry and still have a frequency response up to on the order of 20 Hz. The control signal is applied to the inverting input of operational amplifier 64 of signal conditioner or integrating circuit 66, together with a power factor command signal supplied through resistor 68 from potentiometer 70. Potentiometer 70 is biased negatively to provide a difference or subtraction signal with respect to the positive signal as developed at the outputs of the phase detectors. Signal conditioning is effected by an inverse feedback network consisting of two circuits, one being capacitor 72 connected between the output and inverting input of operational amplifier 64, and the other consisting of a series combination of capacitor

74 and resistor 76 connected between these two points. The feedback network is basically an integrative or lag one. The combination of resistor 76 (approximately 15,000 ohms) and capacitor 74 (approximately 5 MFD) is initially effective (at 0 frequency) to commence providing a lag effect. At about 2 Hz, the lag state commences to diminish as the value of resistor 76 commences to have a dominant effect over capacitor 74. Then at about 20 Hz, capacitor 72 (approximately .68 MFD) commences to be effective to again impose a pronounced lag effect. The resulting signal is a relatively smooth signal representing the integral of the composite outputs of the phase detectors less the command signal. The signal, as used, is represented by the sample signal waveforms S_1 and S_2 as shown in Fig. 4. It is important that while the signals have a relatively smooth and constant level, approximating the average signal value present, the signal must be responsive to signal changes incident to changes in motor loading, typically calling for a signal response upward to approximately 20 Hz. This is achieved by the circuitry shown.

Inasmuch as the control system of the invention has the effect of providing a quite low RMS voltage to motor 10 in its normal running, but unloaded state, and such voltage would be inadequate to provide a starting voltage to the motors, means are provided to insure that the load or power factor control signal is ineffective until the motor is brought up to operating speed. This is accomplished by a delay circuit consisting of capacitor 76 connected to the positive, or non-inverting, input of operational amplifier 64, a resistor 78 connected between this input and ground, and resistor 80 in series with capacitor 76 and +15 volt power supply (as shown). Upon the application of power to motor 10, and at the same time to the bias supply (not shown) providing all bias voltages for the circuitry in Fig. 1, an initial charging current through resistors 78 and 80 is of a value sufficient to override a maximum input applied to the negative input of amplifier 64 for a period of several seconds. Thus, motor 10 may be brought up to operating speed before its input voltage may be effectively reduced in accordance with a control mode as described.

Thyristor triggering signals are developed by the comparison of the control signal (e.g., S_1 and S_2 of Fig. 4) output of operational amplifier 64 and ramp shaped signals r. A ramp signal for each phase is

developed by one of conventional ramp generators 84, 86, and 88, responsive to A-C, C-B, and B-A phase voltages from transformers 38, 42, and 44, respectively. The ramp outputs r of these generators are illustrated by solid line in waveforms ab, b, and c, respectively, of Fig. 4, and are separately applied to conventional comparators 90, 92, and 94, together with a control signal from operational amplifier 64. In operation, a comparator provides a pulse output when the level of the control signal, e.g., dashed line S_1 of Fig. 4, intersects the leading edge of a ramp signal. Thus, as shown, for example, with a control signal S_1 applied to the comparators, there is produced output pulses shown in waveforms d, e, and f of Fig. 4. These pulses, which result in the triggering of the thyristors, as will be described, occur once per cycle, and are thus representative of a half wave mode of operation. The relatively narrow triggering pulses shown as waveforms d, e, and f of Fig. 4 produce relatively short "turn on" times for SCR devices 12, 14, and 16, and thus produce a relatively low RMS input voltage to motor 10. This state of operation will initially have been brought about by phase detectors detecting a downward shift in power factor (by an upward shift in current-voltage phase angle) occurring when motor loading is shifted to a low state. The resulting output signal of operational amplifier 64 will be such as to produce a motor RMS input voltage which brings about an equilibrium between the commanded power factors determined by the bias output of potentiometer 70 and integrated output of the phase detectors.

The actual control of the current "turn on" periods for the thyristors is effected by gates 96, 98, and 100, which pass high frequency signals responsive to the outputs of comparators 90, 92, and 94. Gates 96, 98, and 100 are electronic switches and function to effect gating of the high frequency signal (e.g., 10 KHz) from high frequency oscillator 102 through the primary windings of transformers 104, 106, and 108 to the thyristors. Resistor 110 and diode 112 are connected in series across the primary of each transformer in order to suppress inductive voltages to a safe level consistent with semi-conductive circuitry employed. The secondaries of transformers 104, 106, and 108 are connected, as shown) in series with diode 114 between the gate and cathode of SCR devices 12, 14, and 16. Turn on periods for the thyristors follow, for example, the periods of the

pulse outputs of the comparators (as shown in waveforms d-i). The waveforms marked by waveforms g-i, which are produced by control signal S_2, are illustrative of the turn on periods for a moderately to substantially loaded motor in contrast to pulses shown in waveforms d-f, which are indicative of a slightly loaded or a motor having no load.

Fig. 5 illustrates a modified form of the invention wherein instead of the employment of SCR devices, bi-directional triac switches 110, 111, and 112 are employed. Like components to those of Fig. 1 have like numerical designations. A resistor 113 and capacitor 114 are conventionally connected in series across the power terminals of each of the triac switches in order to stabilize their operation. Since the triac switches are controllable during both half cycles of input power, it is necessary to provide a full wave control, and thus ramp generators 116, 118, and 120 are indicated as being 120 Hz devices. Likewise, phase detectors 122, 124, and 126 are full wave devices, and each is as shown in Fig. 6.

Referring to Fig. 6, the phase detector includes two oppositely phased voltage squaring circuits 128 and 130 and two oppositely phased current squaring circuits 132 and 134. The outputs of voltage squaring circuit 128 and current squaring circuit 132 are summed through resistors 136 and 138 and the sum rectified by diode 140. Similarly, the outputs of voltage squaring circuit 130 and current squaring circuit 134 are summed through a like pair of resistors 136 and 138 and rectified by a diode 140. Finally, the rectified outputs of the squaring circuits appear on the common terminal 142, on which there is connected all phase detector outputs, as will be noted in Fig. 5. These outputs, there being two for each half cycle of input to each phase, appear in Fig. 7, showing that in a time period of one cycle of 60 cycle current, a period of 0.16 seconds, 6 output pulses occur. Thus, there is provided twice as many output pulses as the circuit shown in Fig. 1. By virtue of this higher frequency output, a frequency of 360 Hz compared to 180 Hz for the circuit of Fig. 1, the time constant characteristic of signal conditioning or integrating circuit 150 differs from signal conditioner 66 of the circuit of Fig. 1. Signal conditioner 150 includes three inverse feedback circuits between the output and input of operational amplifier 151, one consisting of capacitor 152, one consisting of capacitor 154 in series with

resistor 156, and one consisting of resistors 158 and 160 and an intermediate capacitor 162 connected to ground. Capacitor 152 typically has a value of .15 MFD, or from .12 to .18 MFD. Capacitor 154 typically has a value of 20 MFD, or from 18 to 22 MFD. Resistor 156 typically has a value of 12,000 ohms, or in the range of from 10K to 15K ohms. Resistors 158 and 160 typically have like values of 18,000 ohms, or in the range of from 16K to 20K ohms, and capacitor 162 typically has a value of 3 MFD, or in the range of from 2 to 4 MFD. The function of these feedback circuits is as follows. Capacitor 152 provides a low pass filter to smooth the square wave feedback control signal. Capacitors 162 and 168 and resistors 156, 158, and 160 provide a lead-lag-lead network required for stabilizing the closed loop control signal.

The output of operational amplifier 151 (Fig. 5) is fed to comparators 90, 92, and 94, which function, as described, for their counterparts in Fig. 1, except that the rate of comparison performed by each is at a 120 Hz rate. The outputs of the comparators otherwise control gates 96, 98, and 120 in the same manner to apply high frequency triggering signals to triacs 110, 111, and 112 during a portion of each half cycle (rather than during them only once each cycle, as in the case of the system shown in Fig. 1) determined by load on motor 10 to effect power control, as otherwise described with respect to Fig. 1.

As a further difference between the systems of Figs. 1 and 5, it is to be noted that instead of the coordinate order of input voltage-current signal inputs to the phase detectors as shown in Fig. 1, the order of the connection of circuitry of Fig. 5 differs. Thus, in Fig. 5, the voltage-current input to the phase detectors is directly relatable in terms of the input phase designations A, B, and C. Accordingly, the voltage input to phase detector 122 is obtained from the A-B phase input, and the current of that phase detector is obtained from sampling the current through the A phase input. Similarly, the B-C phase input voltage applied to phase detector 124 is compared with the current input obtained from current flow through the B phase input. Finally, the C-A voltage input applied to phase detector 126 is compared with a current derived signal input from current flow through the phase C input. Further, the voltage input to each of the phase detectors and ramp generators of Fig. 5 is shifted by

an R-C (resistance-capacitance) circuit consisting of resistor 130, resistor 132, and capacitor 134, which effects an essentially 40° lag in current with respect to voltage. It is found that a 40° phase lag produces the optimum delay of the trigger pulses required for turning on the triacs.

Both of the embodiments of this invention illustrated herein provide a smooth current input control to motor 10 and accomplish a power factor type regulation of input power as a function of loading and without significant motor instability.

THREE PHASE POWER FACTOR CONTROLLER

Abstract

A power control circuit for a three phase induction motor wherein power factors for the three phases are summed to provide a control signal, and this control signal is particularly filtered and then employed to control the duty cycle of each phase of input power to the motor.